Datasheet

APW8811

Based on the ARM®Cortex®-M0

Bluetooth 4.2 Ultra-low Power SoC

Version: 2020.01

1 APW8811: Bluetooth 4.2 Ultra-low Power SoC

1.1 General Description

The APW8811 is an ultra-low power Bluetooth 4.2 SoC based on the 32-bit ARM®Cortex®-M0 core, integrated with high-performance 2.4GHz RF transceiver and rich digital interfaces. With on-chip Balun, there is no need for off-chip impedance matching network and external crystal oscillator load capacitance, which minimize BOM cost and PCB area. A high-efficiency DC-DC step-down converter is integrated to realize ultra-low power consumption.

1.2 Key Features

- Fully qualified Bluetooth Low Energy 4.2 standard
- Based on ARM®Cortex®-M0 core
- 2.4GHz RF transceiver
- 8 channel 1MSPS 10-bit SAR ADC
- Support OTA
- 32MHz and 32.768kHz crystal oscillator
- Built-in buck DC-DC converter
- 64MHz and 32.768kHz RC oscillator
- Quadrature Decoder
- Support ISO7816 interface
- Infrared emitting and receiving
- Communication interface options
  - Master I²C x2
  - Master Three SPI &Four-Wire SPI
  - UART x2
- Digital peripherals
  - PWM x6
  - RTC
- configurable GPIO features
- Serial Wire Debug(SWD) supported

1.3 Applications

- Intelligent wearable
- Smart home
- Remote controller
- Health applications
- HID devices

1.4 Key Parameters

Parameter	APW8811KEU6	APW8811CEU6
Frequency	64MHz	64MHz
Max. TX Power	+4 dBm	+4 dBm
RX Sensitivity	-94dBm	-94dBm
TX Current	4.8 mA@0dBm	4.8 mA@0dBm
RX Current	2.8 mA@0dBm	2.8 mA@0dBm
Sleep Mode Current	2.7μA	2.7μA
Deep Sleep Mode Current	1 μA	1 μA
Flash	512 kB	512 kB
Data RAM	24 kB	32 kB
Supply Voltage	1.8~3.6 V	1.8~3.6 V
GPIO	21	21
Operating Temperature, Tj	-40~+85 °C	-40~+85 °C
Package	5.0 x 5.0 x 1.0 mm	5.0 x 5.0 x 1.0 mm

*Condition: V_{DD}=3V, DCDC enable.

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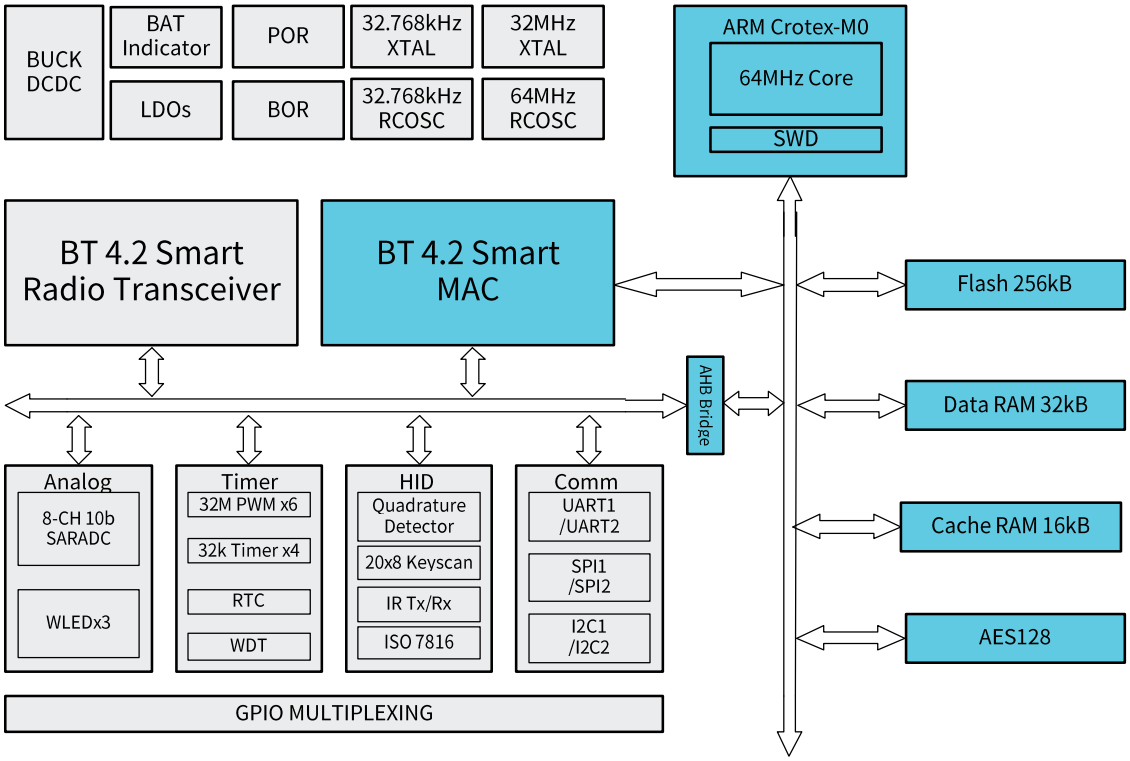
2 Introduction

2.1 Overview

The APW8811 chip is highly integrated with 32-bit ARM®Cortex®-M0 processor, Radio Transceiver, Bluetooth Modem, Bluetooth 4.2 baseband, Flash and SRAM, on-chip Balun and digital interfaces such as SPI/I2C/UART etc. The ARM® Cortex®-M0 processor can operate at the highest clock rate of 64MHz for heavy thread computing applications, and can also operate at lower clock rate for simple data communication purpose. A built-in DCDC converter is integrated to provide full-solution SoC for stand-alone applications such as IoT and wearable devices.

错误!未找到引用源。shows the architecture block diagram of the chip. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

Figure 1.Functional Block Diagram



2.2 Terminology

Table 1. Terminology

Term	Description
GND	Ground
BiDir	Bi-Directional
PWM	Pulse Width Modulation
HID	Human Interface Device
GPIO	General Purpose Input / Output

2.3 Pin Assignment and Signal Description

2.3.1 QFN32 Pin Assignment and Signal Description

Figure 2.QFN32 pin assignments, top view (5mm*5mm)

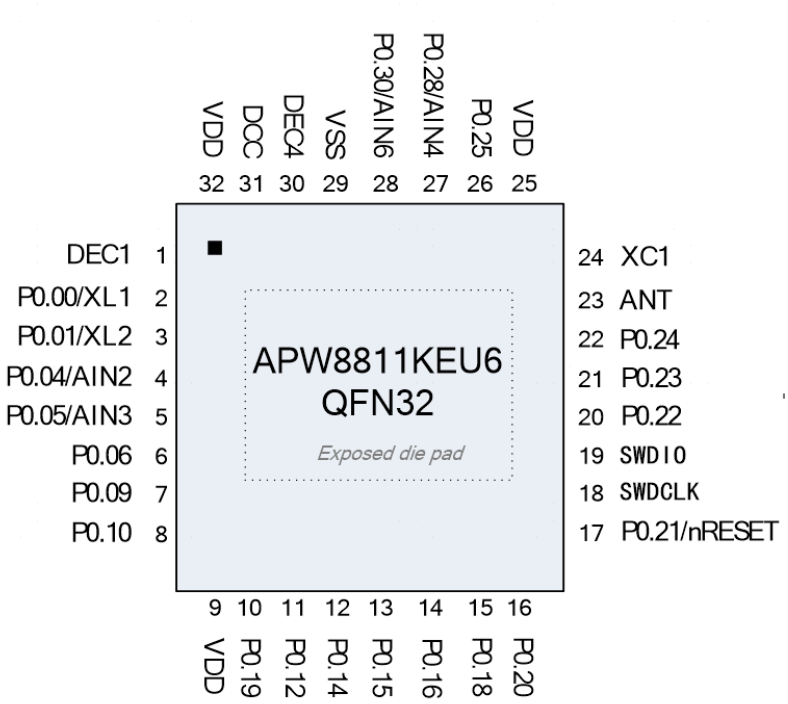


Table 2. QFN32 pin assignments

Pin	Name	Type	Description
Left side of chip			
1	1-Dec	Power	1.1 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC input
5	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC input
6	P0.06	Digital I/O	General purpose I/O
			Capacitive touch
7	P0.09	Digital I/O	General purpose I/O
8	P0.10	Digital I/O	General purpose I/O
Lower side of chip			
9	VDD	Power	Power supply
10	P0.19	Digital I/O	General purpose I/O
11	P0.12	Digital I/O	General purpose I/O
12	P0.14	Digital I/O	General purpose I/O
13	P0.15	Digital I/O	General purpose I/O
14	P0.16	Digital I/O	General purpose I/O
15	P0.18	Digital I/O	General purpose I/O
16	P0.20	Digital I/O	General purpose I/O
Right side of chip			
17	P0.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
18	SWDCLK	Digital input	Serial wire debug clock input for debug
			and programming
19	SWDIO	Digital I/O	Serial wire debug I/O for debug and
			programming
20	P0.22	Digital I/O	General purpose I/O
21	P0.23	Digital I/O	General purpose I/O
22	P0.24	Digital I/O	General purpose I/O
23	ANT	RF	Single-ended radio antenna connection
24	XC1	Analog input	Connection for 32 MHz crystal
Upper side of chip			

Pin	Name	Type	Description
25	VDD	Power	Power supply 1.8~3.6V
26	P0.25	Digital I/O	General purpose I/O
27	P0.28	Digital I/O	General purpose I/O
	AIN4	Analog input	Capacitive touch
			SAADC input
28	P0.30	Digital I/O	General purpose I/O
	AIN6	Analog input	Capacitive touch
			SAADC input
29	VSS	Power	Ground
30	4-Dec	Power	1.25 V power supply, output with 10uF or 4.7uf capacitance
31	DCC	Power	DCDC switch node, connect to DCDC inductance, high current path, keep PCB as wide and short as possible
32	VDD	Power	Power supply 1.8~3.6V
Bottom of chip			
Die pad	VSS	Power Ground pad	Exposed die pad must be connected to ground (VSS), 9 or more via holes are recommended

QFN48 Pin Assignment and Signal Description

Figure 3.QFN48 pin assignments, top view (6mm*6mm)

2.3.2

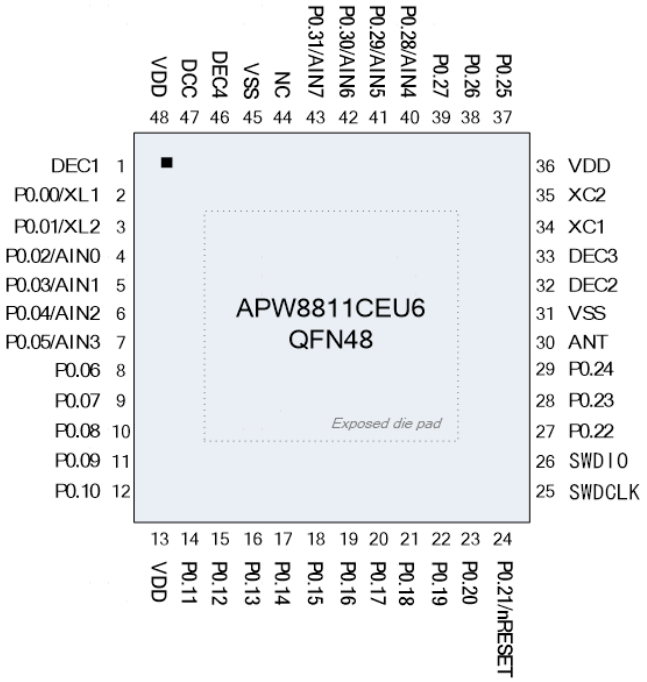


Table 3. QFN48 pin assignments

Pin	Name	Type	Description
Left side of chip			
1	1-Dec	Power	1.1 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.02	Digital I/O	General purpose I/O
	AIN0	Analog input	SAADC input
5	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC input
6	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC input
7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC input
8	P0.06	Digital I/O	General purpose I/O
			Capacitive touch

Pin	Name	Type	Description
9	P0.07	Digital I/O	General purpose I/O
			Capacitive touch
10	P0.08	Digital I/O	General purpose I/O
			Capacitive touch
11	P0.09	Digital I/O	General purpose I/O
12	P0.10	Digital I/O	General purpose I/O
Lower side of chip			
13	VDD	Power	Power supply 1.8~3.6V
14	P0.11	Digital I/O	General purpose I/O
15	P0.12	Digital I/O	General purpose I/O
16	P0.13	Digital I/O	General purpose I/O
17	P0.14	Digital I/O	General purpose I/O
18	P0.15	Digital I/O	General purpose I/O
19	P0.16	Digital I/O	General purpose I/O
20	P0.17	Digital I/O	General purpose I/O
21	P0.18	Digital I/O	General purpose I/O
22	P0.19	Digital I/O	General purpose I/O
23	P0.20	Digital I/O	General purpose I/O
24	P0.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
Right side of chip			
25	SWDCLK	Digital input	Serial wire debug clock input for debug
			and programming
26	SWDIO	Digital I/O	Serial wire debug I/O for debug and
			programming
27	P0.22	Digital I/O	General purpose I/O
28	P0.23	Digital I/O	General purpose I/O
29	P0.24	Digital I/O	General purpose I/O
30	ANT	RF	Single-ended radio antenna connection
31	VSS	Power	Ground
32	2-Dec	Power	1.1 V RF supply with 0.1uf decoupling
33	3-Dec	Power	1.1V simulation supply with 0.1uf decoupling
34	XC1	Analog input	32 MHz crystal oscillator port 1(HFXO)
35	XC2	Analog input	32 MHz crystal oscillator port 2(HFXO)
36	VDD	Power	Power supply 1.8~3.6V
Upper side of chip			

Pin	Name	Type	Description
37	P0.25	Digital I/O	General purpose I/O
38	P0.26	Digital I/O	General purpose I/O
39	P0.27	Digital I/O	General purpose I/O
40	P0.28	Digital I/O	General purpose I/O
	AIN4	Analog input	SAADC input
41	P0.29	Digital I/O	General purpose I/O
	AIN5	Analog input	SAADC input
42	P0.30	Digital I/O	General purpose I/O
	AIN6	Analog input	SAADC input
43	P0.31	Digital I/O	General purpose I/O
	AIN7	Analog input	SAADC input
44	NC		Float
45	V_{SS}	Power	Ground
46	4-Dec	Power	1.25 V power supply, output with 10uF or 4.7uf capacitance
47	DCC	Power	DCDC switch node, connect to DCDC inductance, high current path, keep PCB as wide and short as possible
48	V_{DD}	Power	Power supply, 1.8~3.6V
Bottom of chip			
Die pad	VSS	Power Ground pad	Exposed die pad must be connected to ground (VSS), 9 or more via holes are recommended

3 Operating Specifications

3.1 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
VDD Voltage	V_{VDD}	-0.4	V_{VDD}+0.3	V	
I/O Voltage	V_{DDIO}	-0.4	V_{DDIO}+0.3	V	
Relative Humidity	RH	0	50	%	Non-condensing, Non-biased
ESD	ESD_{HBM}		2	kV	JESD22-A114E Standrad

Notes:

1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.
4. Functional operation under absolute maximum-rated conditions is not implied and should be restricted to the Recommended Operating Conditions.

3.2 Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature	T_A	-40	25	85	°C	
Operating Junction Temperature	T_J	-40	-	85	°C	
Power Supply Voltage	V_{VDD}	1.8	3.3	3.6	V	Buck DCDC Power input supply. Includes overshoot
I/O Supply Voltage	V_{DD}	1.8	3.3	3.6	V	Includes ripples
Regulator Output Voltage	V_{DEC1}	0.9	1.1	1.2	V	Power for internal digital circuit

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Serial Clock Frequency	SPI_CLK	-	-	32	MHz	
	I^2C_SCL	-	4001	10002	KHz	

Note: APW8811KET6 does not guarantee the performance if the operating temperature is beyond the specified limit.

3.3 Thermal Specifications

Table 6. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-40	-	85	°C	
Lead-free Solder Temperature	T_P	-	-	245	°C	Refer to Package Handling Information document

3.4 DC Characteristics

Table 7. DC Electrical Specifications

Parameters	Symbol	Min	Typ.	Max.	Unit	Conditions
DCDC Converter Input Voltage	V_{VDD}	1.8	3.3	3.6	V	
DCDC Converter Output Voltage	V_{Buck_OUT}	1.1	1.25	-	V	
DCDC Converter Output Current	I_{Buck_Out}	-	-	40	mA	Maximum output current under constant output voltage
DCDC Converter Output Ripple	R_{Buck}	-	30	-	mV	Peak to peak
Power Consumption[2]						
TX RF Current @Pout = 0dBm			4.8		mA	@V_{VDD}= 3V with DCDC enable
RX RF Current @Sensitivity level			2.8		mA	@V_{VDD}= 3V with DCDC enable
Supply Current @ Sleep	I_{SLEEP}	-	2.7	-	μA	@V_{VDD}= 3V with DCDC enable
Supply Current @ Deep sleep	I_{PD}	-	1	-	μA	@V_{VDD}= 3V with DCDC enable

Notes:

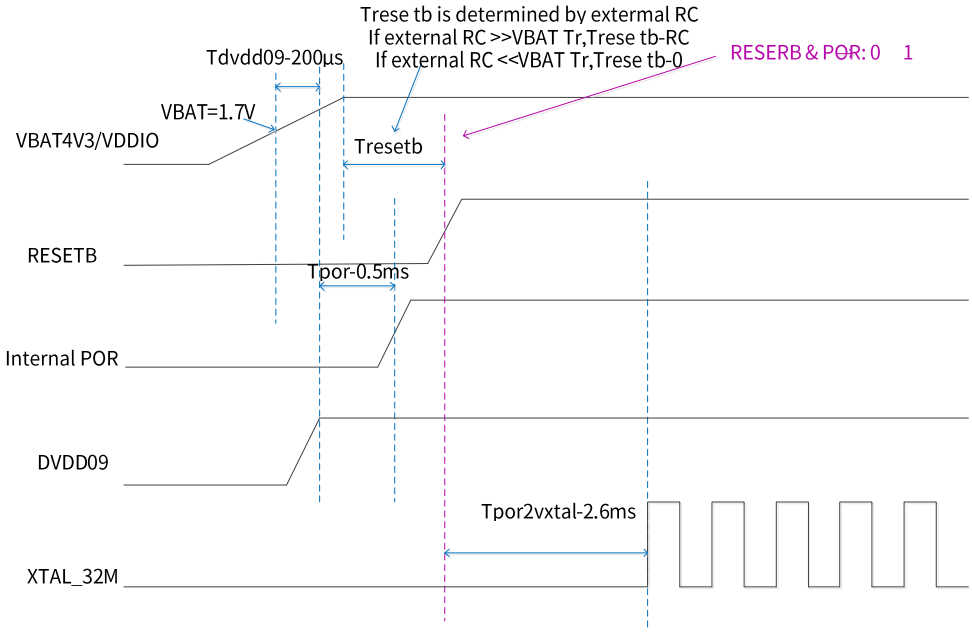
1. Electrical Characteristics are defined under recommended operating conditions.
2. All the parameters are tested under operating conditions: VVDD = 3.0V, DCDC Buck enable mode at T_A = 25°C。

3.5 AC and Timing Characteristics

Power-On Sequence

Figure 4.Power-On Sequence

3.5.1



3.5.2

32MHz Crystal Oscillator

The 32MHz Pierce crystal oscillator is designed for ultra-low power consumption and high stability. The 32MHz oscillator can be trimmed without external capacitors. Two digital controlled trimming loading capacitors are integrated and optimally designed for 10pF XTAL. Digital controlled capacitors could ease and speed up tuning procedure of XTAL frequency accuracy. The simplified schematic of the 32MHz crystal is shown in 0.

Figure 5.32MHz Crystal Oscillator Circuit

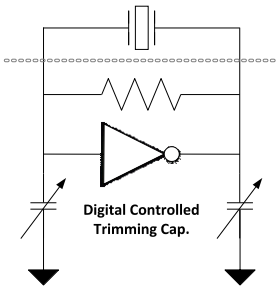


Table 8. 32MHz Crystal Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Crystal Oscillator Frequency	F_{X32M}	-	32		MHz	
Crystal Oscillator Frequency tolerance	F_{X32M_TOL}	-	10	20	ppm	Frequency tolerance depends on XTAL Spec.
Equivalent series Resistor	ESR_{X32M}		30	100	W	
Loading Capacitor	C_{L_X32M}		9		pF	Built in digital controlled trimming loading cap, no external cap needed.
XTAL Drive Power	P_{DRIVE_X32M}			100	uW	
XTAL OSC Start Up Time	T_{START_X32M}		1.5	2.5	ms	

3.5.3 **Notes:** Electrical Characteristics are defined under recommended operating conditions

32.768kHz Crystal Oscillator

The 32.768 kHz oscillator is designed optimally for XTAL with C-Load =12.5pF , and no internal trimming capabilities and 32.768kHz clock is used as the clock source in the Sleep or Power Down modes.

Figure 6.32.768kHz Crystal Oscillator Circuit

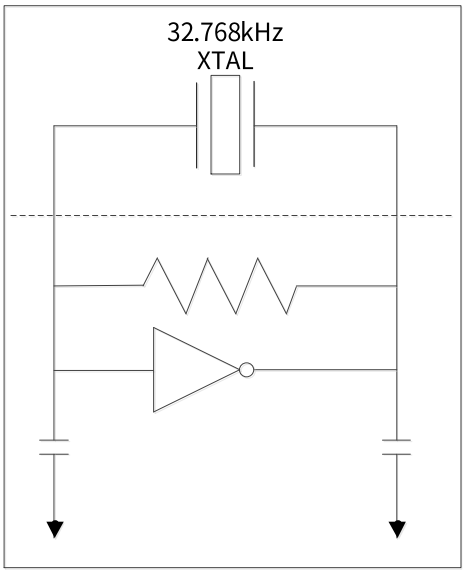


Table 9. 32.768kHz Crystal Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Crystal Oscillator Frequency	F_{X32k}		32.768		kHz	
Crystal Oscillator Frequency tolerance	F_{X32k_TOL}		20		ppm	
Equivalent series Resistor	ESR_{X32k}		50	80	kW	
Load Capacitor	C_{L_X32k}		12.5		pF	Built internal fixed load cap for 12.5pF XTAL
XTAL Drive Power	P_{DRIVE_X32k}			1	uW	
XTAL Start Up Time	T_{START_X32k}		0.3	1	s	

3.5.4

64MHz RC Oscillator

The 64MHz RC oscillator is designed for high speed wake up and high computing power application. Due to characteristic of RC oscillator, calibration is needed before switching to 64MHz RC oscillator mode. The 64MHz RC oscillator starts much faster than the 32MHz crystal oscillator.

Table 10. 64MHz RC Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Oscillator Frequency	F_{RC64M}		32		MHz	
RC Oscillator Frequency tolerance	F_{RC64M_TOL}		1	5	%	
Oscillator Start Up Time	T_{ST_RC64M}		2.5		us	

Notes: Electrical Characteristics are defined under recommended operating conditions

32.768kHzRC Oscillator

3.5.5 The 32.768kHz RC oscillator is designed for low cost applications without additional 32.768kHz XTAL. Due to characteristic of RC oscillator, calibration is needed before switching to 32.768kHz RC oscillator mode.

Table 11. 32.768kHz RC Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Oscillator Frequency	F_{RC32k}		32.768		kHz	
RC Oscillator Frequency tolerance	F_{RC32k_TOL}		2		%	
RC Oscillator Frequency tolerance, Calibrated	F_{RC32k_TOL}		250	500	ppm	Calibration needed before switching to RC oscillator mode
Start Up Time	T_{START_X32K}		100		us	

Notes: Electrical Characteristics are defined under recommended operating conditions

3.6 RF Specifications

Transmitter RF Specification

Table 12. Transmitter Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Range	FR_{TX}	2402	-	2480	MHz	
Max. Output Power	$P_{O,MAX}$	-		4	dBm	
Default Output Power	$P_{O,DEF}$		0		dBm	
Output Power Adjust Range	$P_{O,ADJ}$	-30		4	dBm	2dBm/step
Output Power Variation	$P_{O,VAR}$		2		dBm	n
TX 20dB Bandwidth	BW_{20dB}			1150	kHz	
1st Adjacent Channel Power	P_{AJC1}			-20	dBc	
2nd Adjacent Channel Power	P_{AJC2}			-40	dBc	
Delta F1 Frequency Deviation	$\Delta f1_{AVG}$	225		275	kHz	
Delta F2 Frequency Deviation	$\Delta f2_{AVG}$	185			kHz	
AVG Delta F2/ Delta F1	Δf_{AVG}	0.8				Δf2AVG/Δ f1AVG
Frequency Offset	F_{OFFSET}	-150		150	kHz	
Carrier Frequency Drift	CF_{DRIFT}			50	kHz	
Carrier Frequency Drift rate	CF_{DRIFT_Rate}			20	kHz/50μs	
2nd Harmonics Power Level	Har_{2nd}			-40	dBm	@Pout = 0dBm
3rd Harmonics Power Level	Har_{3rd}			-45	dBm	@Pout = 0dBm

Notes: Electrical Characteristics are measured under BLE specification and

3.6.1

recommended operating conditions

Receiver RF Specification

Table 13. Receiver Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
3.6.1 Frequency Range	FR_{RX}	2402		2480	MHz	
Maximum Input Power	RX_{MAX}		0		dBm	With PER <30.8%
Ideal Signal Sensitivity	SEN_{IDEAL}		-94		dBm	
Dirty Signal Sensitivity	SEN_{DIRTY}		-92		dBm	
C/I and Selectivity						
C/I Co-Channel	C/I_{CO}		9		dB	
C/I Adjacent +1MHz	C/I_{1M}		-1		dB	
C/I Adjacent +2MHz	C/I_{2M}		-38		dB	
C/I Adjacent≧ +3MHz	C/I_{3M}		-48		dB	
C/I Image Channel	C/I_{IMG}		-25		dB	
C/I Image+1M Channel	C/I_{IMG+1M}		-35		dB	
Inter-Modulation Performance						
IMD performance	IMD		-24		dBm	3rd, 4th and 5th offset channel
Blocking Performance						
Blocking 30~2000MHz	$P_{BLK\_30\sim2000MHz}$	-10			dBm	
Blocking 2003~2399MHz	$P_{BLK\_2003\sim2399MHz}$	-30			dBm	
Blocking 2484~2997MHz	$P_{BLK\_2484\sim2997MHz}$	-30			dBm	
Blocking 3000MHz~12.75GHz	$P_{BLK\_3\sim12.75GHz}$	-10			dBm	

Notes: Electrical Characteristics are measured under BLE specification and recommended operating conditions

4 Design References

4.1 Application Schematics

4.1.1 APW8811KEU6 Reference Application Circuit

Figure 7.APW8811KEU6 Reference Application Circuit (32.768k xtal is optional)

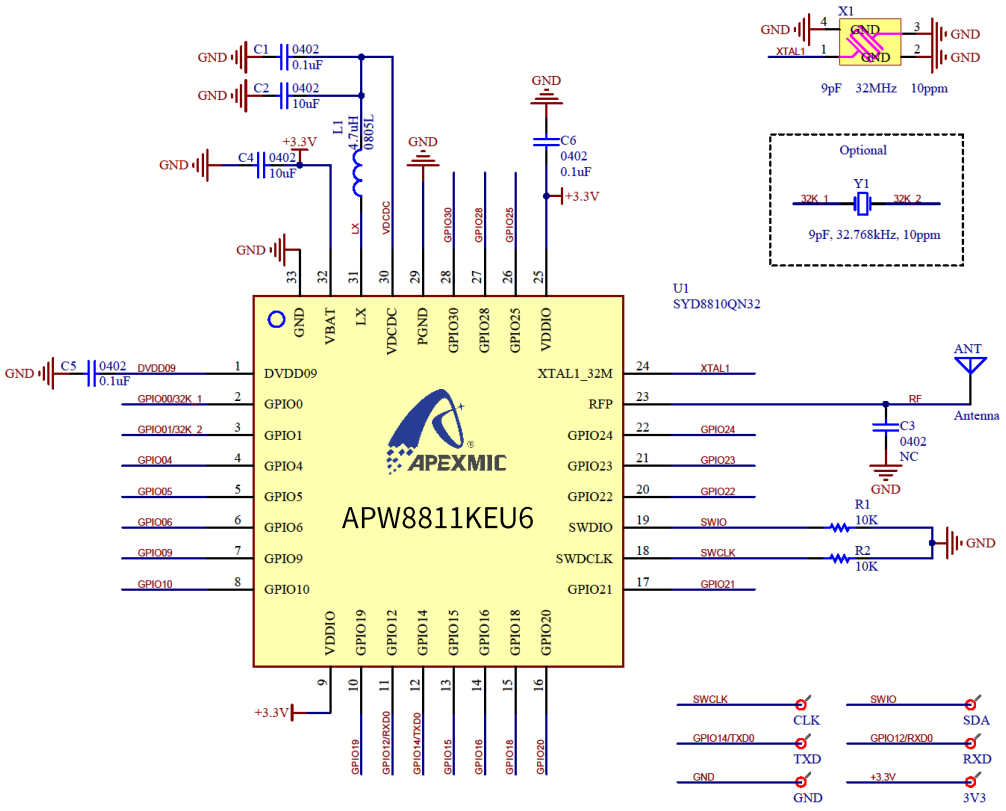


Table 14. BOM of APW8811KEU6

Designator	Value	Description	Footprint
C4, C5	100 nF	Capacitor, X5R, ±20%	402
C9	4.7 µF	Capacitor, X5R, ±20%	0603 or 0402
C10	10 µF recommended	Capacitor, X5R, ±20%	603
L2	4.7 µH	Inductor, IDC,min = 30 mA, ±20%	603
U1	APW8811KEU6	ULP Bluetooth low energy SoC	QFN48
X1	32 MHz	32 MHz, CL = 10 pF, Tol: ±10ppm	3225
X2 (optional)	32.768 kHz	32.768 kHz, CL = 12.5 pF, Tol: ±20 ppm	3215

Figure 8.APW8811CEU6 Reference Application Circuit (32.768k xtal is optional)

4.1.2

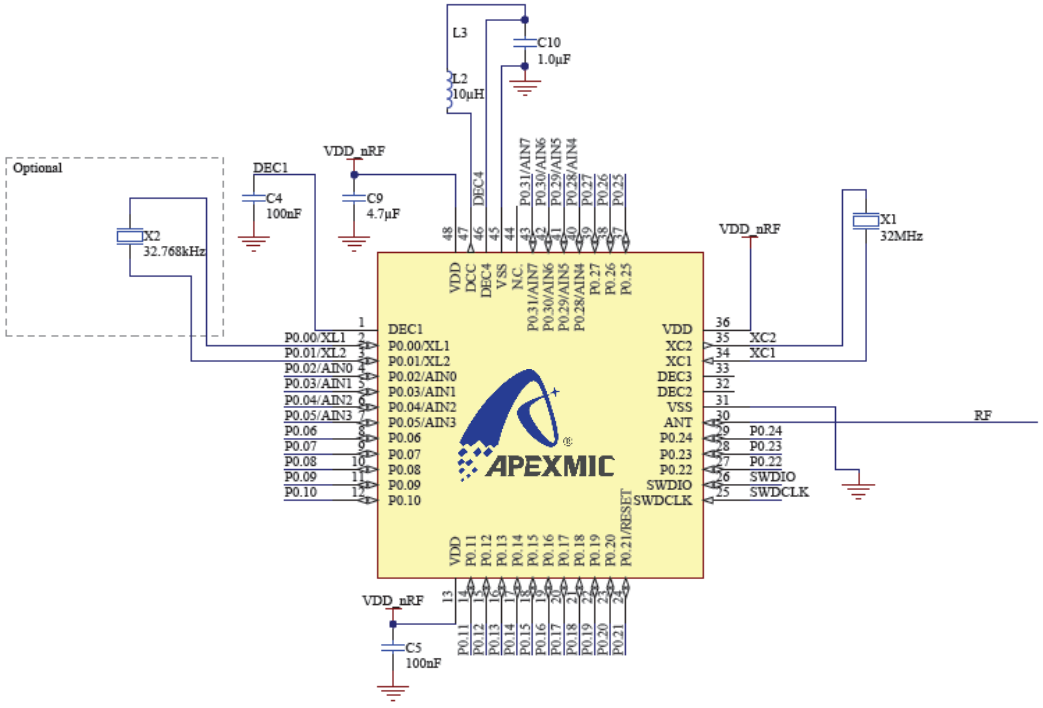


Table 15. BOM of APW8811CEU6

Designator	Value	Description	Footprint
C4, C5	100 nF	Capacitor, X5R, ±20%	402
C9	4.7 µF	Capacitor, X5R, ±20%	0603 or 0402
C10	10 µF recommended	Capacitor, X5R, ±20%	603
L2	4.7 µH	Inductor, IDC,min = 30 mA, ±20%	603
U1	APW8811CEU6	ULP Bluetooth low energy SoC	QFN48
X1	32 MHz	32 MHz, CL = 10 pF, Tol:±10ppm	3225
X2 (optional)	32.768 kHz	32.768 kHz, CL = 12.5 pF, Tol: ±20 ppm	3215

4.2 Layout Design Guidelines

Precaution: PCB layout is extremely important to minimize parasitical capacitance and improve RF performance.

The following layout guidelines are recommended to achieve optimum

performance.

1. Make sure RF 50-ohm trace is with GND continuation.
2. Place the DCDC inductor close to the DCC pin. Keep the traces short and wide enough.
3. Place the decoupling capacitor C10 close to the DEC4 PIN.
4. Route PIN45 VSS to gnd plane by VIA（4layer PCB）, or route PIN45 VSS to bottom layer by VIA (2layer PCB), DO NOT connect PIN45 VSS to top layer gnd; ** PIN45 VSS is dirty DCDC gnd.
5. Place passive crystal oscillator as close as possible to the oscillator pins to reduce the parasitic capacitance and the interference to other circuits.
6. Ensure that the ground plane under the oscillator and its components are in good quality.
7. Avoid long connections to the passive crystal and also to the load capacitor which may create a large loop on the PCB.
8. Do not route any digital-signal lines on the opposite side of the PCB under the RF trace and crystal area.
9. Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from crystal/analog/RF connections as possible.
10. Place at least 9 ground VIAs directly under QFN thermal PAD for good grounding and thermal dissipation.

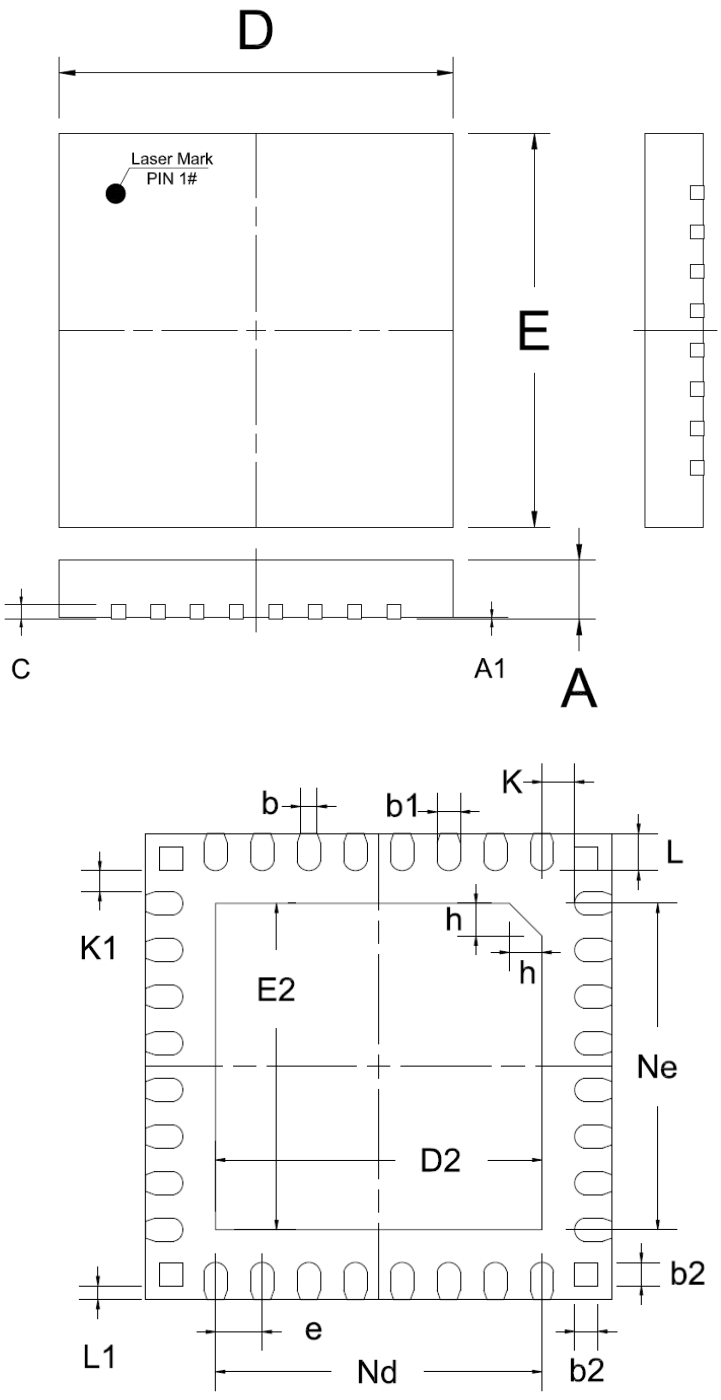
5 Mechanical Specifications

5.1 APW8811KEU6 Packaging

Mechanical Dimension

Figure 9.APW8811KEU6 Package Outline Diagram and Dimension

5.1.1



Apexmic	MILLMETER		
	MIN	MON	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.2	0.25	0.3
b1	0.18REF		
b2	0.2	0.25	0.3
c	0.203REF		
D	4.9	5	5.1
D2	3.4	3.5	3.6
e	0.50BSC		
Nd	3.50BSC		
Ne	3.50BSC		
E	4.9	5	5.1
E2	3.4	3.5	3.6
L	0.35	0.4	0.45
L1	0.15REF		
h	0.3	0.35	0.4
K	0.35REF		
K1	0.225REF		

Package Marking

Refer to Figure 10 for the code marking location on the device package.

Figure 10. Package Marking

5.1.2

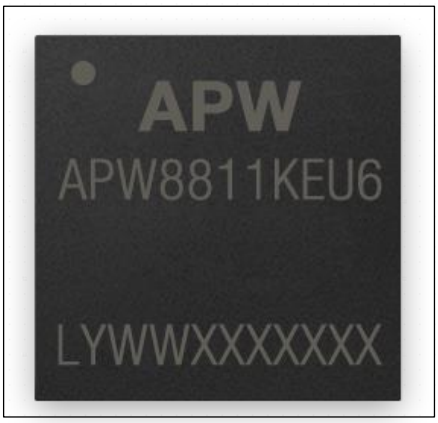


Table 16. Code Identification

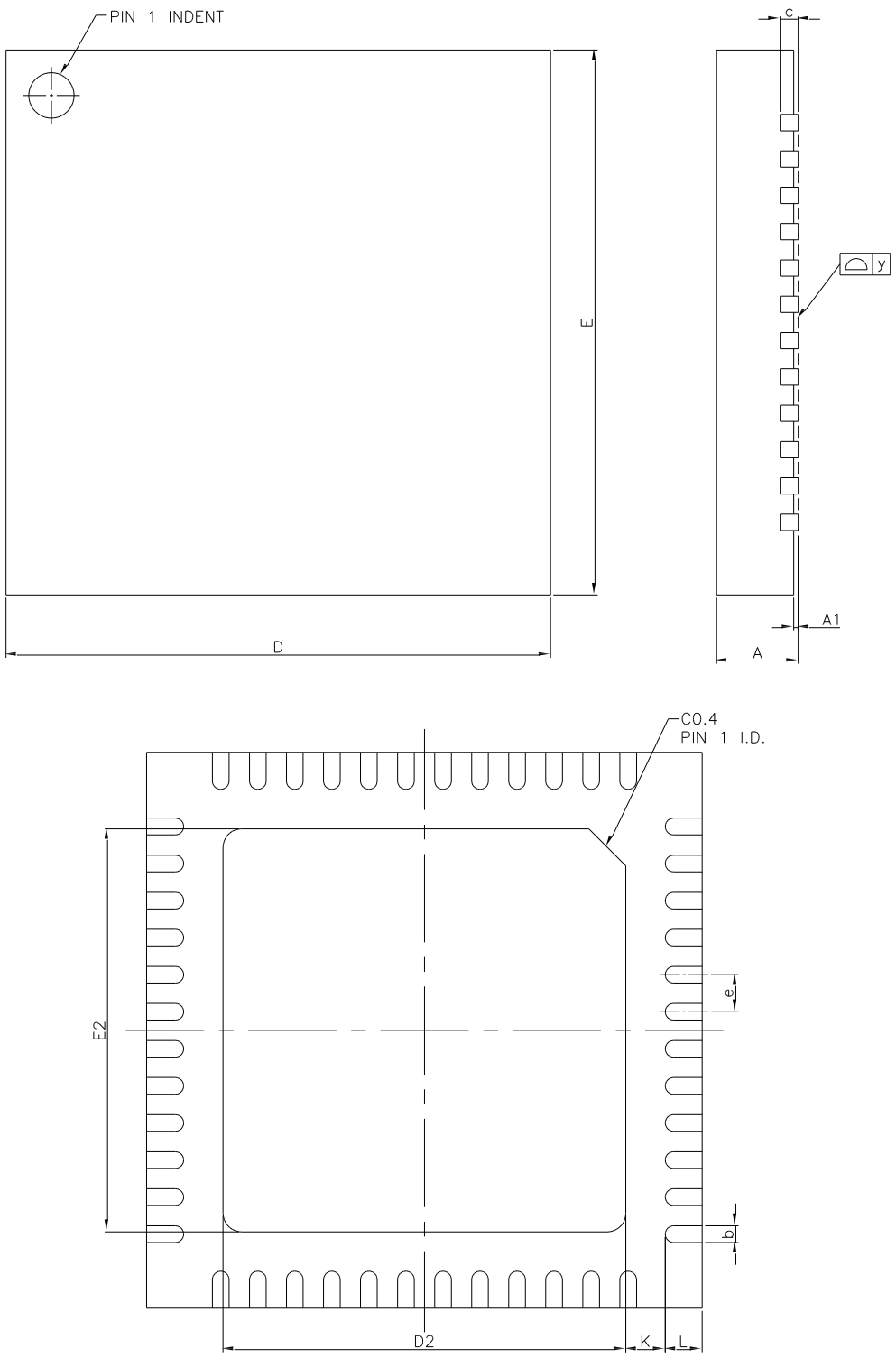
Marking	Description
LYWWXXXXXXX	APW8810KEU6 Date Code
	Y: Assembly year
	e.g. (Yearly 2018) -> 8
	WW: Assembly week
	e.g. (Weekly 16) -> 16
	XXXXX: NO.
	e.g. 433CE12

5.2 APW8811CEU6 Packaging

Mechanical Dimension

5.2.1

Figure 11. APW8811CEU6 Package Outline Diagram and Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	- - -	0.20REF	- - -
D	5.90	6.00	6.10
D2	4.30	4.35	4.40
E	5.90	6.00	6.10
E2	4.30	4.35	4.40
e	- - -	0.40	- - -
K	- - -	0.425REF	- - -
L	0.350	0.400	0.450
y	0.00	- - -	0.075

5.2.2 Package Marking

Refer to Figure 12 for the code marking location on the device package.

Figure 12. Package Marking

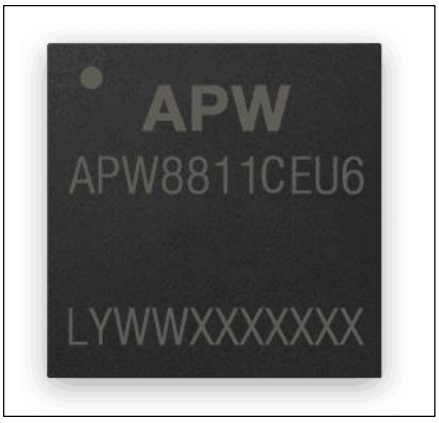


Table 17. Code Identification

Marking	Description
LYWWXXXXXXX	APW8810CEU6 Date Code
	Y: Assembly year
	e.g. (Yearly 2018) -> 8
	WW: Assembly week
	e.g. (Weekly 16) -> 16
	XXXXX: NO.
	e.g. 433CE12

6 Power States & Sequence

Table 18. Operation Mode

State	Functional Description
Deep sleep	All power supplies are off except retention cell and I/O for pin wake-up. All clocks are gated.
	System can be woken up by configured external pin. When it happens, APW8811 series of chips are reset from boot-up state.
Sleep	Active clocks (32MHz xtal and 64MHz RCOSC) are off, and the sleep clock (32.768kHz) remain working. Certain engines' power are off.
	Two types of sleep modes are provided in APW8811. When CPU uses internal 64MHz RC clock, it can set CPU sleep mode independently and woken up by timer or Bluetooth interrupts. When CPU uses 32MHz crystal clock together with Bluetooth, it follows Bluetooth sleep mode aligning to connection interval.
Standby	This is the default state after power-up. All clocks are working but the RF is inactive.
TX	This mode is entered when Bluetooth link-layer determines to send transmission packets.
RX	This mode is entered when Bluetooth link-layer determines to receive an incoming packet.

7 System Description

7.1 ARM®Cortex®-M0

Cortex®-M0 processor is the smallest ARM processor available. It provides ultra-low power consumption and minimal code of the processor to enable developers to achieve 32-bit performance. With its friendly architecture, users can develop applications easily and fast.

APW8811 series supports dynamic clock technology for various applications ranging from 8MHz to 32MHz. The CPU clock can be configured to use internal 64MHz RC clock or 32MHz crystal clock. When using RC clock, MCU can run independently with Bluetooth link-layer and switch on and off at users' discretion. When using 32MHz crystal clock, it should follow the working period of Bluetooth (the Bluetooth working

period can be determined by MCU).

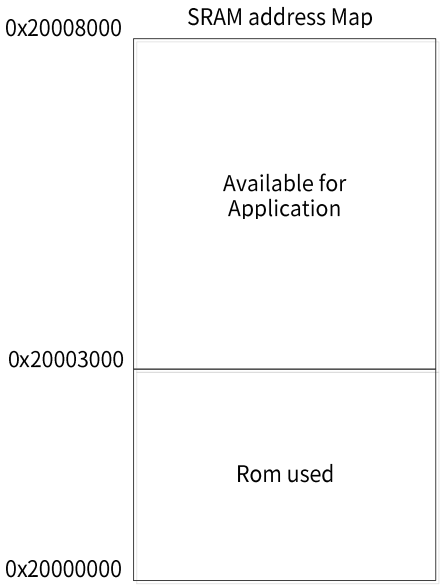
SWD (Serial-Wire Debug) is supported for powerful debug and trace features with two connection pins.

APW8810KET6 has 24KB ROM for boot-up and BLE protocol stack, 512kB flash for profile/application, and 32kB exchange/data SRAM.

7.2 Memory

- ROM: 32kB internal ROM is for the Boot code and Bluetooth Low Energy protocol stack firmware.
- Data RAM: 32kB Data RAM is integrated, 12kB will be used up by ROM(BLE stack), 20kB is available for application.
  - 0x2000 0000 ~ 0x2000 3000 (12kB) is used by ROM.
  - 0x2000 3000 ~ 0x2000 8000 (20kB) is available for application
- Flash: 512kB flash is integrated for code and firmware storage.

Figure 13. Data SRAM Address Map



7.3 Bluetooth Low Energy Core

The Bluetooth Low Energy Core of APW8811 is SIG Qualified. It is fully compliant with Bluetooth Smart v4.2 slave-role controller and provides qualified features as below:

- Bluetooth low energy stack: All layers up to GATT including (PHY, LL, HCI, L2CAP, GAP, SM, ATT/GATT)
- Slave-Role Link layer
  - Slave-required PDU types
  - Encryption/Decryption
- L2CAP
  - Slave connection update
  - Attribute channel
  - Security channel
- GAP/ATT/GATT: Mandatory protocols
- Security Management
  - Key generation and passing
  - Automatic security engine
- DTM: For RF qualification
- Profile configuration
  - Initialization
  - Flexibility and testability

7.4 Radio Transceiver

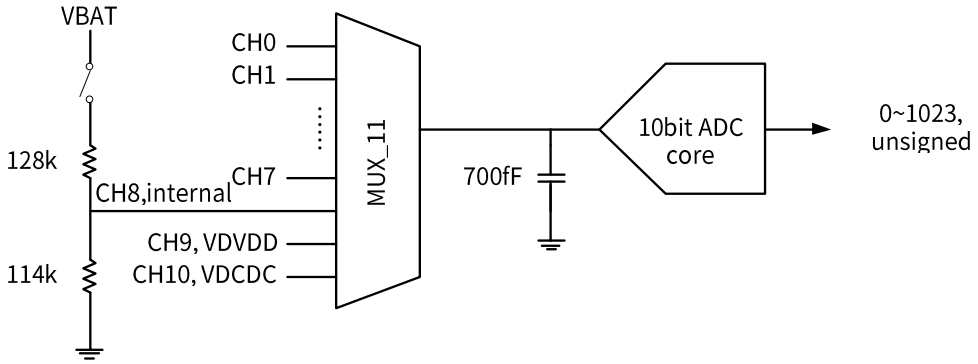
The APW8811 series integrates high performance 2.4GHz radio transceiver for Bluetooth radio specification. With the built-in on-chip balun, APW8811 does not need external balun circuit to minimize BOM. The integrated high efficiency PA can transmit up to +4dBm RF power for class 2 operation, while the integrated low-IF receiver can provide excellent sensitivity up to -94dBm and outstanding ACI interference rejection capability for good receptivity in the complex working environment of 2.4ghz ISM band.

7.5 General Purpose ADC (SAADC)

The APW8811 series integrates a low power 10-bit general purpose Analog-to-Digital Converter (GPADC) with 1MHz sampling rate. It can operate as a 9-channel ADC by switching the GPADC input. One channel is for internal Battery Voltage detection (VVDD), while the other eight are

configured to monitor eight GPIOs. For better accuracy, internal reference voltage calibration is preferred. Sensing applications as battery monitoring, temperature resister, analog signal sampling could be applied with this GPADC.

Figure 14. GPADC Internal Channel MUX and Resister Divider Configuration



7.6 Power Management

The APW8811 series integrates a power management unit for handheld or wearable devices with DCDC converter. The DCDC converter transforms battery voltage to a lower/higher internal voltage with minimal power loss. The DCDC converter could provide excellent power efficiency with adaptive loading current setting. The DCDC Buck converter can be bypassed when the supply voltage drops to the lower limit of the voltage range, and external DCDC converter is also supported. It can provide power solution for one-cell Lithium-Ion, one-cell or two serial alkaline battery applications where the output voltage is adjustable, 1.15V~3.6V.

7.6.1 Buck Converter

Higher performance DCDC Buck converter would bring up better battery life time. To ensure longest battery life, Buck converter has an optional bypass mode under light load current. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. For better conversion efficiency, DC resistance (RDC) should be less than 0.25ohm.

Figure 15. DCDC Buck Converter Configuration

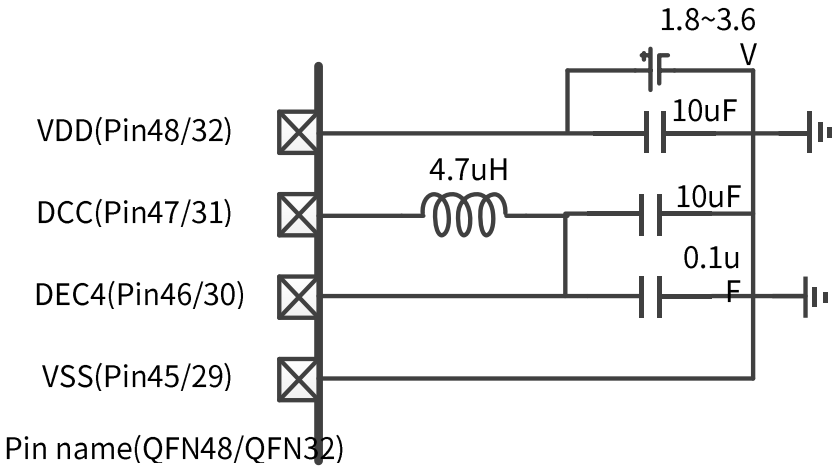


Table 19. Buck Converter Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Voltage	$V_{In,Buck}$	1.8	3.3		V	
Output Voltage	$V_{DCDC,Buck}$	1.8	3.3		V	
Converting Efficiency	Eff_{Buck}		88		%	@20mA Loading current
Maximum Load Current	$I_{Load,Buck}$			40	mA	
Output Ripple Voltage	$V_{RIPPLE,Buck}$		30		mV	

7.7 GPIO

APW8811 series offers maximum 32 GPIOs and 2 SWD debug ports (SWDCLK, SWDIO). SWDCLK and SWDIO pins should be pulled low during APW8811 booting procedure.

GPIO features:

- Configurable output drive strength
- Optional internal pull-up resistors
- Configurable input polarity
- Support both high or low level triggered pin wake-up
- Each GPIO can be individually mapped to any digital function for

layout flexibility

- Hardware de-bounced GPIO

7.8 Timer

APW8811 series provides 4 low speed Timers, Timer0~Timer3 are running with 32.768KHz clock from 32.768KHz crystal oscillator clock or 32KHz RC clock. Timer interrupt can wakeup CPU from sleep mode. Timer3 is reserved for Rom Code. APW8811 also provides a high speed timer.

7.8.1 Low Speed Timer

APW8811 series provides 4 low speed timers with 32-bit width.

Timer0~Timer3 are running with 32.768kHz clock from XTAL or LPO.

Timer interrupt can wakeup CPU from sleep mode. Timer3 is reserved for Rom Code, not for external application.

7.8.2 High Speed Timer

The high speed timer works with the 32MHz RC clock, which has 16-bit width for high speed and accurate timing application. Two operating modes are provided, one -time or continuous, an interrupt to MCU can be triggered by timer at the end of period.

7.9 Real Time Clock (RTC)

APW8811 series offers an RTC timer for real time clock application.

7.10 Watch Dog Timer (WDT)

APW8811 series offers one 16-bit countdown watchdog timer for supervisor purpose. It also runs at 32.768kHz clock for maximum 2sec supervisor time to execute system reset due to a hardware fault or program error.

7.11 SW Encryption

APW8811 series offers 48bits encryption key for flash code protection.

7.12 AES Encryption Engine

The AES engine accelerates the algorithm calculations that are needed for

implementing the user defined security algorithm. The AES encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

8 Peripheral

8.1 Hardware Keyscan

APW8811 series provides an 8x20 keyscan decoder for maximum 8 rows and 20 columns. The row and column could be assigned in specified IO for flexible configuration and layout.

When key is pressed, the keyscan circuit would auto scan the defined matrix and report to firmware in FIFOs.

8.2 Quadrature Decoder

APW8811 series provides a quadrature decoder for HID application. It could detect quadrature encoder signals and report to firmware in FIFOs. The decoder support sleep wakeup function.

8.3 PWM

APW8811KEU6 integrates 4 channels low speed PWM (32.768KHz) and 6 channels high speed PWM (the highest 32 MHZ).

APW8811CEU6 integrates 3 channels low speed PWM (32.768KHz) and 3 channels high speed PWM (the highest 32 MHZ).

8.3.1

High speed PWM

APW8811KEU6 integrates 6 channels high speed PWM with max. 32MHz clock, APW8811CEU6 integrates 3 channels high speed PWM with max. 32MHz clock. The characteristics are as following:

- The period can be configured (four channels are the same).
- Each channel can be configured its ratio and initial polarity independently.
- The period, duty cycle can be update dynamically (be in effect next

period)

- The pulse could to be center-aligned or edge-aligned.

Figure 16. Center-aligned PWM

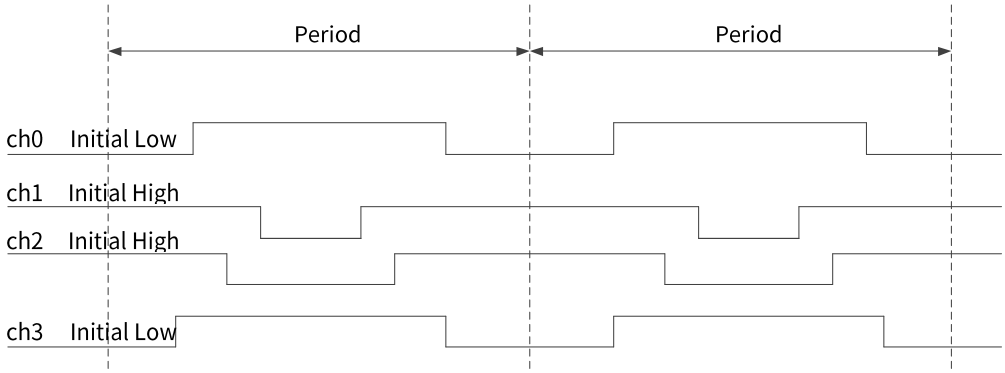
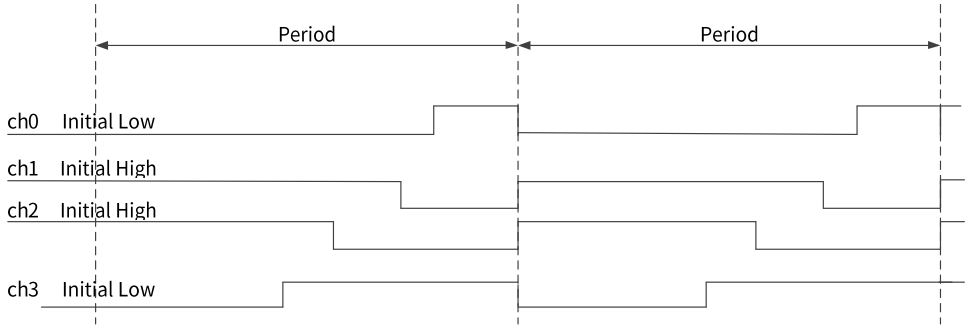


Figure 17. Edge-aligned PWM

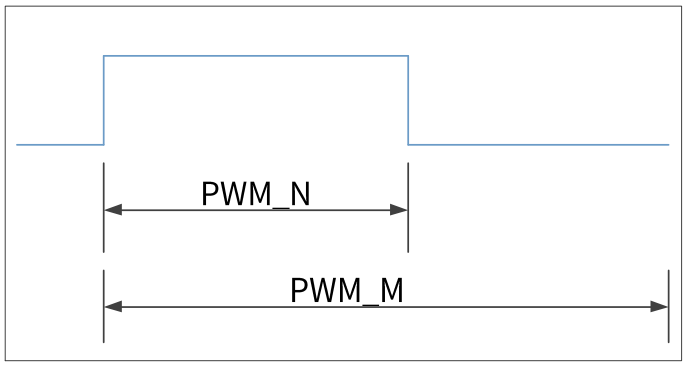


8.3.2

Low speed PWM (LED Controller)

APW8811KEU6 integrates 4 adjustable PWM generators while APW8811CEU6 integrates 3, and the both can be controlled by individual register and could be mux out at three different GPIOs. The minimum positive or negative width of PWM is 1/32ms and flexible setting ranges from 1 to 255 steps. Buzzer or LED dimming could be controlled by PWM signal with pre-defined PWM duty.

Figure 18. PWM Timing Setting Diagram



APW8811 series integrates LED controller which provide general On-OFF mode and Breathing light mode. The minimum LED on width is 1/32s with max 255 steps. LED ON-OFF repetition times could be configured as continuous or 1~127 times. Register table has setting description details. T1, T2, T3 are 8-bit width control register with minimum step 31.25ms.

For Breathing light mode, min, max, T4 are 8-bit width control register with minimum step 0.5ms. The sp is defined as breath mode speed with 4-bit width control resister with minimum step, 31.25us.

Figure 19. LED ON-OFF Setting Diagram

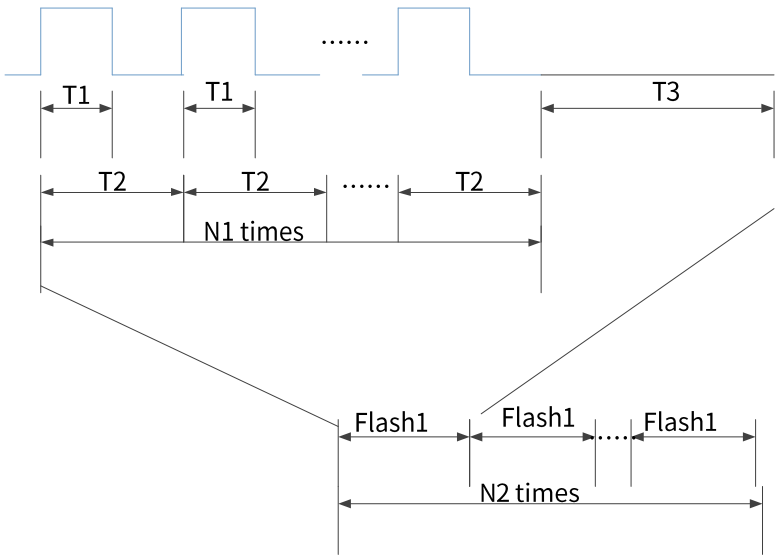
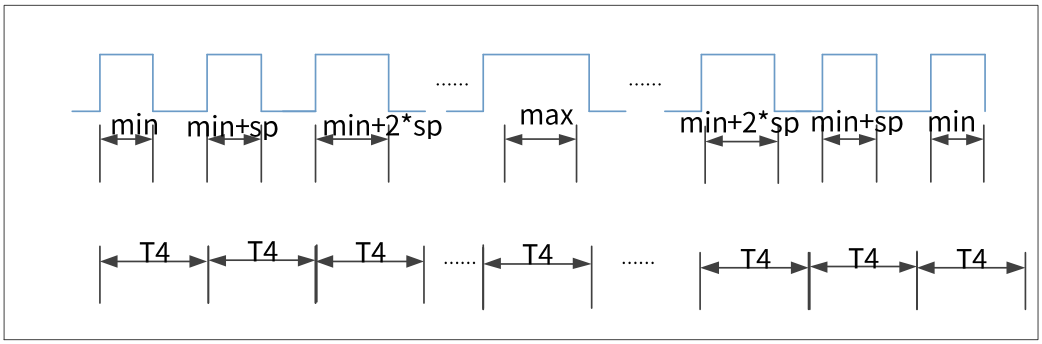


Figure 20. LED Breathing Light Setting Diagram



9 Interfaces

9.1 UART

The APW8811 series has two sets of UART interface (UART0, UART1) for serial asynchronous communication between devices. UART-0 has CTS/RTS hard flow control for option. Data frame configuration is as eight (8) data bits, with parity bit, and one (1) stop bit shown figure below.

Figure 21. UART Data Frame

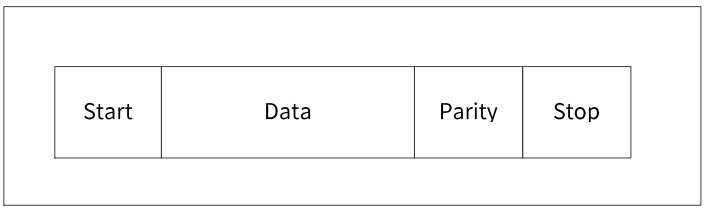


Table 20. UART Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Baud Rate	BR	1200		921600	bps	
Baud Rate Accuracy	BR_{ACCU}			3	%	

9.2 I²C

The APW8811 series has two sets of I2C interface (I2C_0, I2C_1) for 2-wire bi-directional communication between devices. The I2C supports wide range of data rate from 31.25kHz to 1000kHz in register controls. Multiple Read modes are supported as current read, random read, and sequential read. Write mode also support byte write and page write.

Figure 22. I²C Control Byte Format

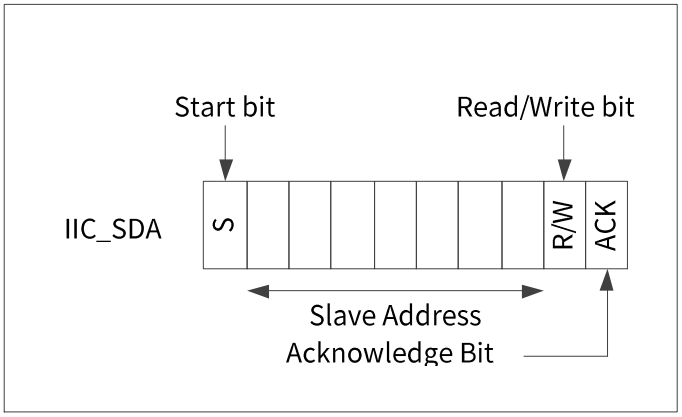


Figure 23. I²C Byte Write Format

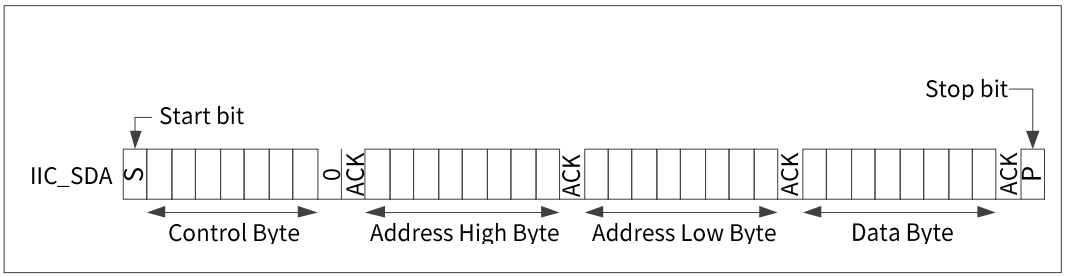


Figure 24. I²C Page Write Format

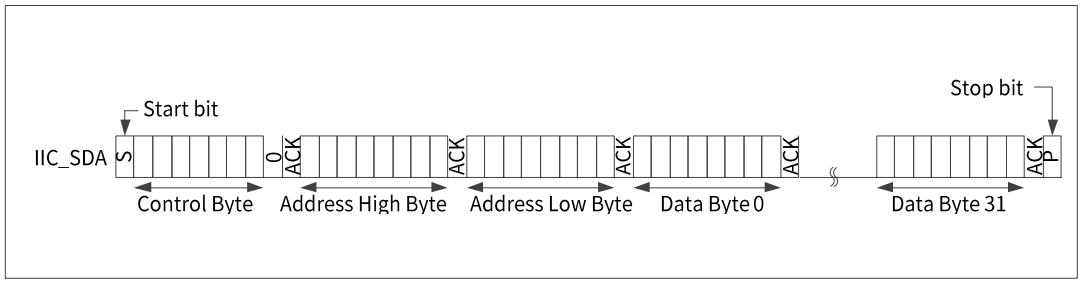


Figure 25. I²C Current Read Format

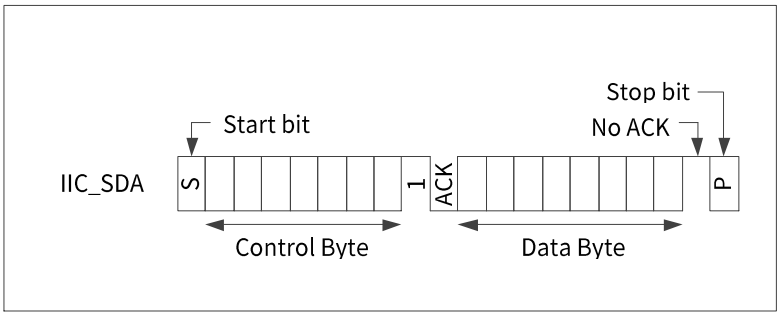


Figure 26. I²C Random Read Format

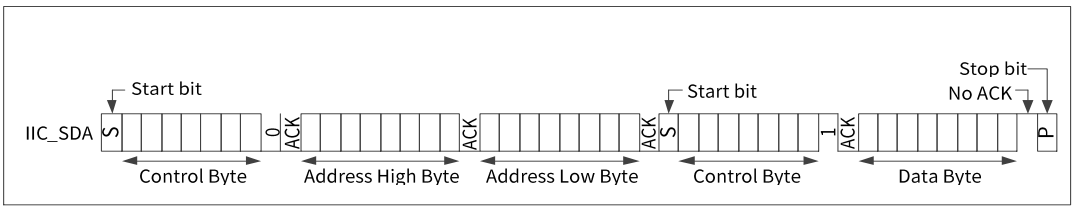
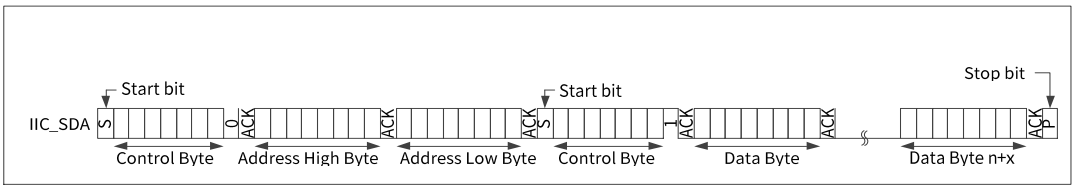


Figure 27. I²C Sequential Read Format



9.3 SPI

The APW8811 series provides two configurations of SPI interfaces. One is four wire SPI, as CSN (chip select), SCLK (clock), SDI (MOSI data) and SDO (MISO data)and the other is two or three wire SPI interface as CSN (chip select) – optional, SCLK (clock), SDIO (bi-directional Data). These two configurations are for master operation only, slave mode is not supported.

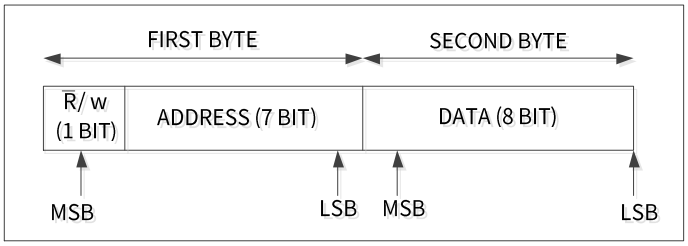
9.3.1 Packet Formats

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has bit-7 as its MSB to indicate data direction. The second byte contains the data.

Figure 28. Four-wire or Three/Two-wire SPI Transmission Protocol



Write Operation

9.3.2

A write operation is always initiated by the APW8811 series and consists of two bytes, which the data is going from the host controller to the device. The first byte contains the 7 bits address and has a “1” as its MSB to indicate data direction. The second byte contains the full 8 bits data. The communication is synchronized by SCLK. The APW8811 series changes SDIO or SDI on the falling edges of SCLK and the device reads SDIO or SDI on the rising edges of SCLK.

Figure 29. Four-wire SPI Write Operation

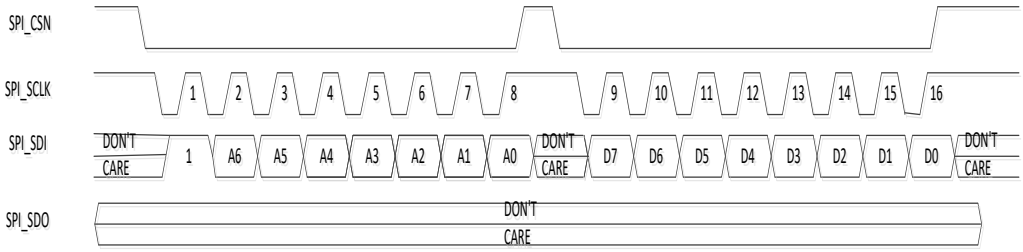
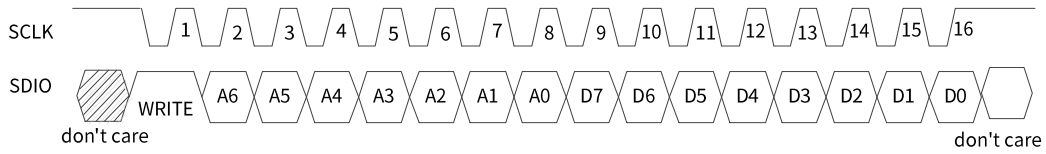


Figure 30. Three/Two-wire SPI Write Operation



9.3.3

Read Operation

A read operation is initiated by the host controller and consists of two bytes. The first byte contains 7-bit address specified by APW8811 and has a “0” as its MSB to indicate data direction. The second byte contains the full 8 bits data and is driven by the slave device. This communication is synchronized by SPI_SCLK. For three/two-wire SPI, SDIO is changed on the

falling edges of SCLK and is read on every rising edge of SCLK. APW8811 release SDIO bus and handover the control of SDIO bus to the device on the falling edge of last address bit.

Figure 31. Four-wire SPI Read Operation

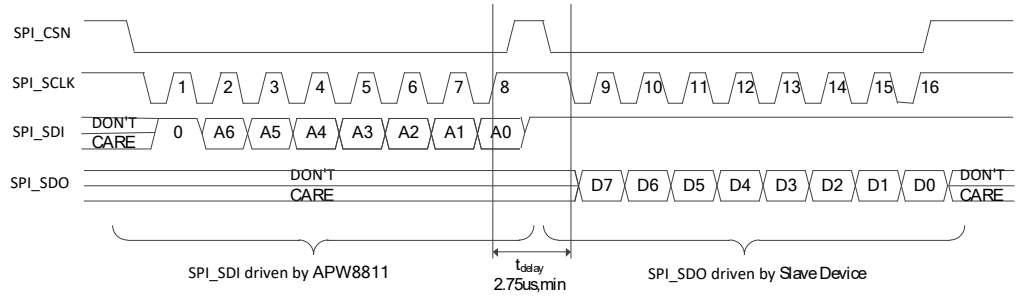
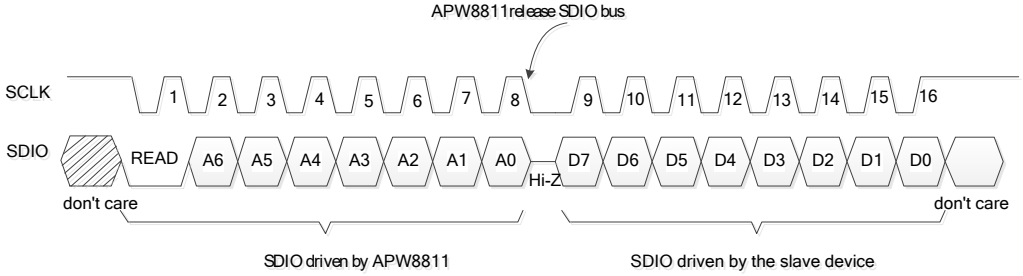


Figure 32. Three/Two-wire SPI Read Operation



9.4 ISO-7816-3

APW8811 series integrates one Smart Card Controller supports asynchronous 3V smartcards. The device is controlled by an ISO 7816-3 interface and is capable of card activation, deactivation, cold/warm reset, ATR parsing and data exchange.

- Compliant to ISO/IEC 7816-3: 1997
- Supports FIFO 8 bytes
- Interrupt report
- Flexible clock frequency and baud rate
- Parity/error check and resend
- T=0 protocol
- Wait time configuration

- ATR wait time
- Reset time
- Guard time

Figure 33. Function block of ISO7816

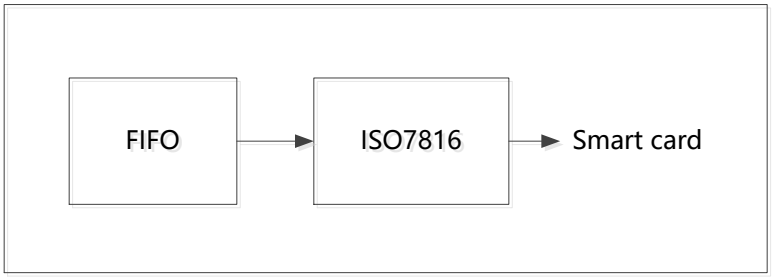


Figure 34. Activation, Cold Reset and ATR

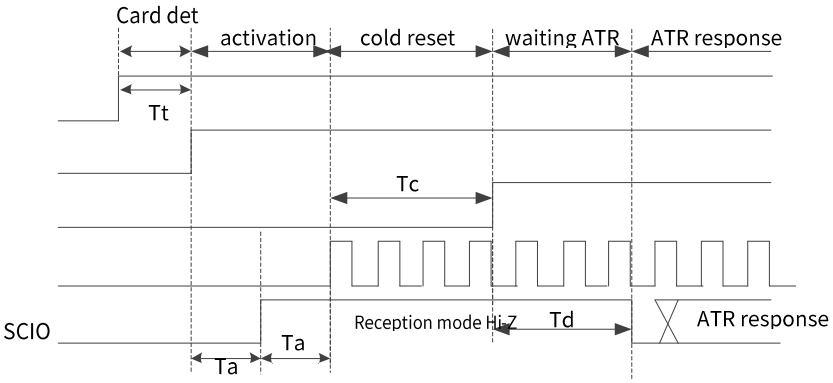
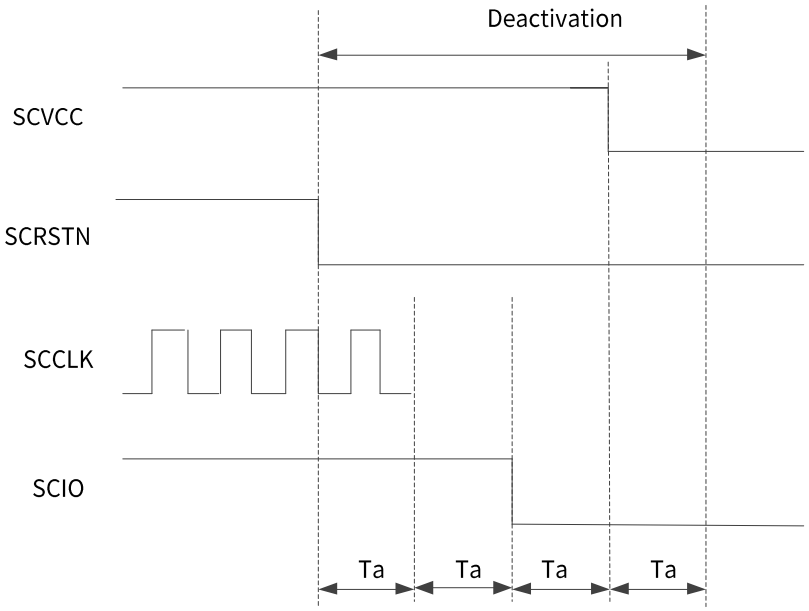


Figure 35. Deactivation Sequence



9.5 IR Transmitter and Receiver

APW8811 series integrates an IR transmitter and Receiver for remote controller applications.

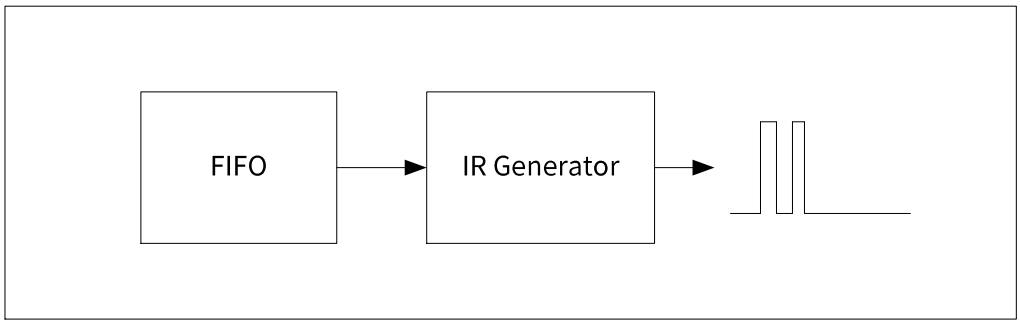
IR Transmitter

9.5.1

The Infrared generator provides a flexible way of transmitting any IR code used in remote controls. It has an efficient message queue where users can describe the waveform of a specific IR command in just a few bytes independently from the protocol.

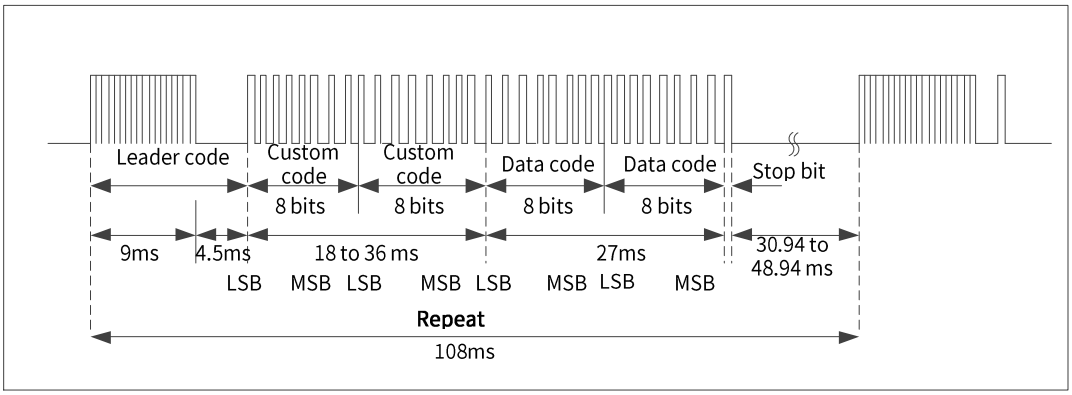
- Flexible carrier frequency and duty cycle.
- Flexible MARK and SPACE.
- Any IR remote control protocol.
- Supported 8 commands message queue in the FIFO.
- Interrupt report

Figure 36. Function block of IR Generator



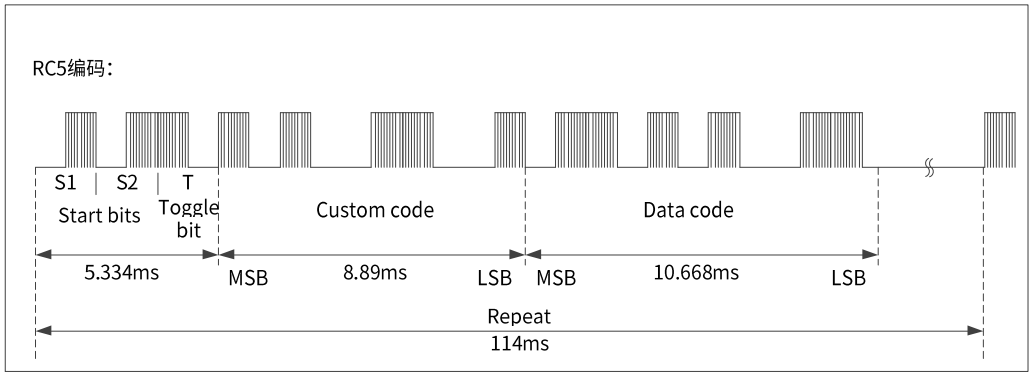
NEC code:

Figure 37. Waveform format of NEC code



RC5 code:

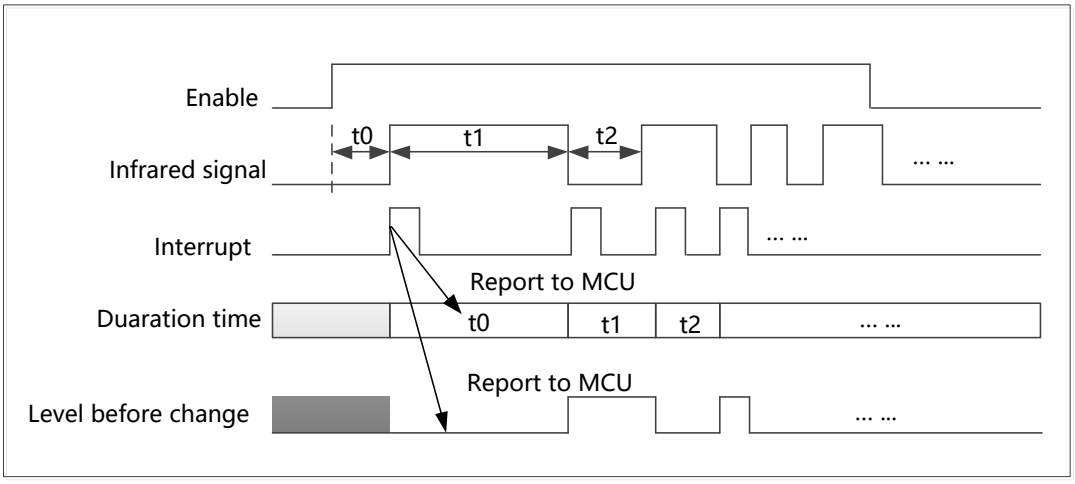
Figure 38. Waveform format of RC5 code



IR Receiver

9.5.2 APW8811 series offer Infrared receiver can detect level change of infrared signal. When detect a level change, the receiver will trigger an interrupt to report MCU that the signal’ s level and duration time prior to the signal change for algorism learning.

Figure 39. IR Receiver



10 Ordering information

Part number	Package	Packing	Minimum Order Quantity
APW8811KEU6	QFN 5mmx5mm 32-Pin	Tape Reel	3K
APW8811CEU6	QFN 6mmx6mm 48-Pin	Tape Reel	3K

11 Document Revision History

Revision Number	Date	Description
1	3rd Jan. 2020	